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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,106	09/09/2003	Cyril Cabral JR.	FIS920030195US1	2105

32074 7590 10/08/2004

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EXAMINER	
SMOOT, STEPHEN W	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 10/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,106	CABRAL ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-20 and 27-30* is/are rejected.

7)☒ Claim(s) *5 and 21-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9-9-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 09 September 2003.

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (see paragraph [0015]). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign mentioned in the description:

450 in Fig. 4 (see paragraph [0031], last sentence).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character not mentioned in the description:

405 in Fig. 4.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified

and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities:

In paragraph [0051], last sentence, change "910" to --920-- because the sidewalls have already been designated as reference number 920 in paragraph [0049], last sentence; and

In paragraph [0053], second sentence, change "650" to --750-- because reference number 750 is used to designate the gate dielectric in Figs.7-10 (see paragraph [0043], last sentence).

Appropriate correction is required.

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification needs to be amended to provide antecedence for the originally filed claim 4.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 27-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 27 recites the limitation "said spacers" in line 3.

There is insufficient antecedent basis for this limitation in claim 27.

Claim 28 is rejected under 35 U.S.C. 112, second paragraph, because it depends on claim 27.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-2, 6-8, 10-11, 14-18, 20, 27-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US 2002/0058374 A1).

Referring to Figs. 2A-2F, Figs. 3A-3D, paragraphs [0041] to [0047], and paragraphs [0054] to [0060], Kim et al. disclose a method of forming metal gates that includes the following features:

- A dummy gate oxide layer (25) is formed on the surface of a semiconductor substrate (21) as shown in Fig. 2C;
- A dummy gate polysilicon layer (26) is formed on the dummy gate oxide layer (25) as shown in Fig. 2C;
- The dummy gate polysilicon layer (26) and the dummy gate oxide layer (25) are patterned into dummy gates (60) as shown in Fig. 2D;
- Nitride spacers (28) are formed on the sidewalls of the dummy gates (60) as shown in Fig. 2E;
- An insulating interlayer (30) is formed over the semiconductor substrate (21) including the dummy gates (60) and then polished back by CMP until the dummy polysilicon layer (26) is exposed as shown in Fig. 2F;
- The dummy polysilicon layer (26) and the dummy gate oxide layer (25) are then removed by etching techniques to form grooves (32a, 32b) as shown in Fig. 3A;
- A gate insulating layer (37) and a first metal layer (38) are then sequentially formed over the semiconductor substrate (21) to line the grooves (32a, 32b) with the first metal layer (38) in contact with the gate insulating layer (37) as shown in Fig. 3B;
- The first metal is formed by CVD and can be tantalum, tungsten, or titanium;

- A portion of the first metal layer (38) is then exposed to a nitridation step as shown in Fig. 3C to form a metal nitride layer (38a) (e.g. tantalum nitride, tungsten nitride, and titanium nitride) on the first metal layer (38); and
- A second metal layer (40) is then formed on the metal nitride layer (38a) to completely fill the grooves (32a, 32b) and layers 40, 38a, 38, 37 are then etched back or polished back until the insulating interlayer (30) is exposed as shown in Fig. 3D.

These are all of the limitations set forth in claims 1-2, 6-8, 10-11, 14, 17, 20, 27-29 of the applicant's invention.

Regarding claims 15-16, the dummy gate oxide layer (25) as shown in Figs. 2C-2F is thicker than the gate insulating layer (37) as shown in Figs. 3B-3D.

Regarding claim 18, Kim et al. further disclose a first metal thickness that ranges from 200 to 400 angstroms (i.e. 20 nm to 40 nm) and a second metal thickness that ranges from 3000 to 5000 angstroms (i.e. 300 nm to 500 nm) (see paragraphs [0056] and [0059]).

Regarding claim 30, the structure resulting from the above method taught by Kim et al. as shown in Fig. 3D and described in paragraphs [0056] to [0059] has all of the structural features set forth in claim 30 of the applicant's invention. Namely, a PMOS field effect transistor with a gate insulator (37), a first metal layer (38) contacting the gate insulator (37), a metal nitride layer (38a) (i.e. a diffusion barrier) formed on the first metal layer (38), and a second metal layer (40) formed on the metal nitride layer (38a), with all of these layers formed between two spacers (28).

10. Claims 1-3, 8, 10-12, 18, 20, 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Ng et al. (US 6,410,376 B1).

Referring to Figs. 2, 6, 11, 13-16, 20-21 and column 2, line 39 to column 4, line 40, Ng et al. disclose a method of forming metal gates that includes the following features:

- A pad oxide layer (18) is formed on the surface of a preferably monocrystalline silicon semiconductor substrate (10) as shown in Fig. 2;
- Dummy nitride gates (40) are formed on the pad oxide layer (18) as shown in Fig. 6;
- Spacers (48) are formed on the sidewalls of the dummy gates (40) as shown in Fig. 11;
- A dielectric layer (52) is formed over the semiconductor substrate (10) including the dummy gates (40) and then polished back by CMP until the dummy gates (40) are exposed as shown in Figs. 13-14;
- The dummy gates (40) are removed to form gate openings as shown in Fig. 15 by etching with hot phosphoric acid;
- A gate dielectric layer (53) and a first diffusion barrier layer (54) are then sequentially formed over the semiconductor substrate (10) to line the gate openings with the first diffusion barrier layer (54) in contact with the gate insulating layer (53) as shown in Fig. 16;

- The first diffusion barrier layer (54) can be titanium nitride or tantalum nitride (i.e. a metal compound) and is deposited by ALCVD;
- A second diffusion barrier layer (64) is deposited on the first diffusion barrier layer (54) in a PMOS area thereby lining the corresponding gate opening as shown in Fig. 20; and
- A metal layer (66) that can be tungsten is then formed on the second diffusion barrier layer (54) to completely fill the gate opening corresponding to the PMOS area as shown in Fig. 20; and
- Layers 66, 64, 54, 53 are planarized by CMP until the dielectric layer (52) is exposed as shown in Fig. 21

These are all of the limitations set forth in claims 1-3, 8, 10-12, 20, 27-28 of the applicant's invention.

Regarding claim 18, Ng et al. further disclose that the first diffusion barrier layer (54) has a thickness that ranges from 150 to 200 angstroms (i.e. 15 nm to 20 nm) (see column 4, lines 3-5) and the metal layer (66) as shown in Fig. 20 is much thicker than the diffusion barrier layer (54).

11. Claims 1, 6-11, 17, 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Abiko (US 2001/0038136 A1).

Referring to Figs. 5, 6A-6F and paragraphs [0059] to [0066], Abiko discloses a method of forming metal gates that includes the following features:

- A dummy insulation film (42) is formed on the surface of a semiconductor substrate and a dummy gate electrode (41) is formed on the dummy insulation film (42) as shown in Fig. 6A;
- The dummy gate electrode (41) can be polysilicon (see paragraph [0051]);
- Side wall insulation films (33 in Fig. 5) are formed on the sidewalls of the dummy gate electrode (41) as shown in Fig. 6A;
- An insulation film (36) is formed outside the side wall insulation films (33 in Fig. 5) as shown in Fig. 6A;
- The dummy gate electrode (41) and the dummy insulation film (42) are then removed to form an opening as shown in Fig. 6B;
- A gate oxide film (39) is then formed in the opening as shown in Fig. 6B;
- A titanium nitride film (43) (i.e. a metal compound) is then formed over the semiconductor substrate to line the opening with the titanium nitride film (43) in contact with the gate oxide film (43) as shown in Fig. 6C;
- A laminated barrier metal film (44) comprising a titanium underlayer and a titanium nitride overlayer is deposited on the titanium nitride film (43) as shown in Fig. 6E;
- A metal gate electrode (32) that can be tungsten is then formed on the laminated barrier metal film (44) to completely fill the opening as shown in Fig. 6F; and
- The metal gate electrode (32) can be planarized to the level of the insulation film (36) by CMP (see paragraph [0056]).

These are all of the limitations set forth in claims 1, 6-9, 11, 17, 27-28 of the applicant's invention.

Regarding claim 10, the laminated barrier metal film (44) can optionally be a single titanium nitride layer (see paragraph [0064]).

12. Claims 1-3, 11-12, 14, 17-20, 29-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Madhukar et al. (US 6,794,281 B2).

Referring to Figs. 6A-6F and column 4, line 63 to column 5, line 35, Madhukar et al. disclose a method of forming metal gates that includes the following features:

- An oxide film (161) is formed on the surface of a semiconductor substrate (102) and polysilicon replacement gate structures (160) with sidewall spacers are formed on the oxide film (161) as shown in Fig. 6A;
- A CVD oxide film (162) is blanket deposited over the semiconductor substrate (102) including over the polysilicon replacement gate structures (160) and is then polished back until the polysilicon replacement gate structures (160) are exposed as shown in Fig. 6B;
- The polysilicon replacement gate structures (160) and underlying oxide film (161) are then removed by etching to form openings in the CVD oxide film (162) as shown in Fig. 6C;
- A gate oxide layer (108) and a platinum layer (110) are then sequentially formed over the semiconductor substrate (102) to line one of the openings with the

platinum layer (110) in contact with the gate oxide layer (108) as shown in Fig. 6E;

- A tantalum nitride layer (114) is then deposited on the platinum layer (110) and a tungsten layer (116) is then deposited on the tantalum nitride layer (114) as shown in Fig. 6E; and
- Regarding the diffusion barrier limitation of claims 1, 29, it is well known in the semiconductor art that tantalum nitride is capable of functioning as a diffusion barrier layer (see for example Ng et al. - column 4, lines 3-6, 23-33).

These are all of the limitations set forth in claims 1-3, 11, 14, 17, 29 of the applicant's invention.

Regarding claim 12, the semiconductor substrate (102) is typically single crystal silicon (i.e. a bulk semiconductor substrate) (see column 2, lines 8-10).

Regarding claims 18-19, Madhukar et al. further disclose a platinum layer (110) thickness that is less than 100 angstroms (i.e. less than 10 nm) (see column 3, lines 53-55) and a tungsten layer (116) thickness as shown in Fig. 6F that is much thicker than the platinum layer (110).

Regarding claim 20, the platinum layer (110) is preferably deposited by CVD (see column 2, lines 58-66).

Regarding claim 30, the structure resulting from the above method taught by Madhukar et al. as shown in Fig. 6F and described in column 5, lines 9-26 has all of the structural features set forth in claim 30 of the applicant's invention. Namely, a field effect transistor with a gate oxide (108), a first metal layer (110) contacting the gate

insulator (108), a metal nitride layer (114) (i.e. a diffusion barrier) formed on the first metal layer (110), and a second metal layer (116) formed on the metal nitride layer (114), with all of these layers formed at least partially between two spacers.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 2002/0058374 A1) as applied to claim 2 above, and further in view of Ng et al. (US 6,410,376 B1).

As shown above, Kim et al. anticipate claim 2 of the applicant's invention. Kim et al. also anticipate the further limitation to claim 3 set forth in claim 4 of the applicant's invention because they teach that the work function can be changed by varying the amount of nitrogen dopant that is used during the nitridation step (see paragraph [0060]). However, Kim et al. are silent regarding the constituents used in their second metal layer and, accordingly lack a material from the group as set forth in claim 3 of the applicant's invention. Ng et al. teach that a metal gate with a diffusion barrier layer (64

in Fig. 21) that may be titanium nitride or tantalum nitride can be used with a metal core layer (66 in Fig. 21) that can be tungsten (see column 4, lines 22-40).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. and Ng et al. in order to use tungsten, as taught by Ng et al., as the second metal of Kim et al. Kim et al. recognize that their second metal layer should have a low resistance (see paragraph [0059]) and tungsten is known in the semiconductor art as a low resistivity metal.

15. Claim 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 2002/0058374 A1) as applied to claim 1 above, and further in view of Lee (US 5,430,320).

As shown above, Kim et al. anticipate claim 1 of the applicant's invention. However, Kim et al. lack the further limitation to claim 1 set forth in claim 13 of the applicant's invention, which is a semiconductor region that includes a polycrystalline semiconductor film or an amorphous semiconductor film. Lee teaches an MOS thin film transistor that includes a polysilicon layer (42), a gate insulating layer (44) and a metal gate electrode (45) (see Fig. 3 and column 6, line 57 to column 7, line 40).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the teachings of Kim et al. in order to apply their metal gate formation method to thin film transistors that utilize a polysilicon active layer as taught by Lee. Lee recognizes that thin film transistors are used in active matrix LCDs for controlling the operation of each pixel.

Allowable Subject Matter

16. Claims 5, 21-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

17. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not teach or suggest, in combination with the other claim limitations, a method of forming a gate structure that includes forming a metal-containing gate with a sequentially formed first layer, diffusion barrier layer, and second layer in an opening formerly occupied by a sacrificial gate, wherein the first layer is deposited using a carbonyl of a metal (e.g. $W(CO)_6$) as a deposition precursor.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Grivna et al., Moriwaki et al., Hsu et al., and Pan et al. teach methods of forming multilayered metal-containing replacement gates. Buchanan et al. and Xi et al. teach methods of forming tungsten gates using tungsten carbonyl as a source material.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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sws

Stephen W. Smoot
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Art Unit 2813